为乐电气，让科技助人为乐

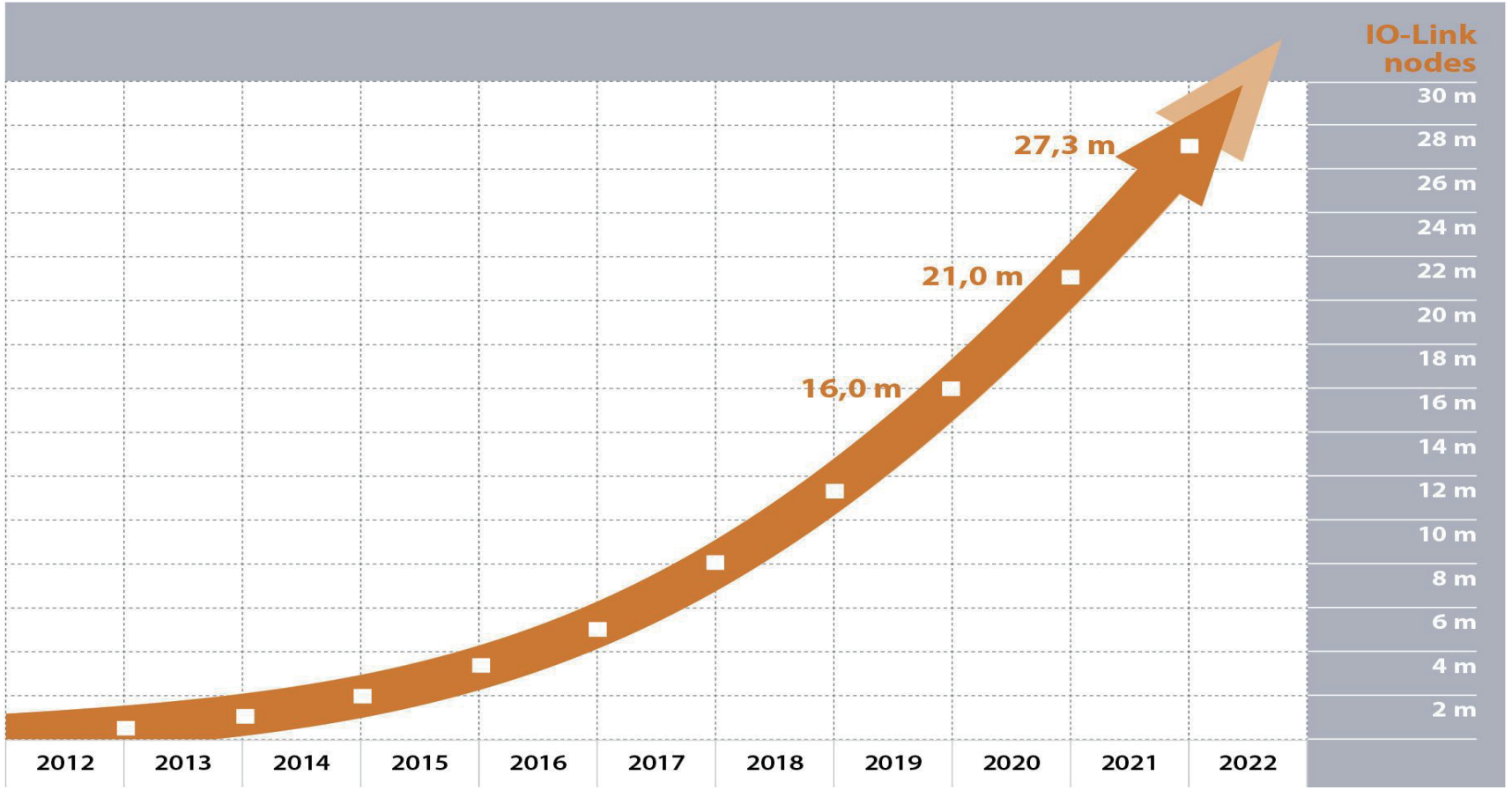
企业官网/website：www.velledq.com

IO-Link解决方案

2023.08

目 录

IO-Link市场增长迅速

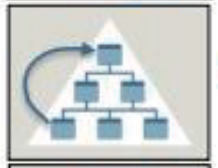


数据来源： www.io-link.com

IO-Link释放传感器的所有潜能

- IO-Link设备以低成本，提供简单的信号外，以及更多诊断，事件，识别，参数信息。

- 减轻了PLC的负荷。 规则，算法和知识库都在传感器和服务器上。



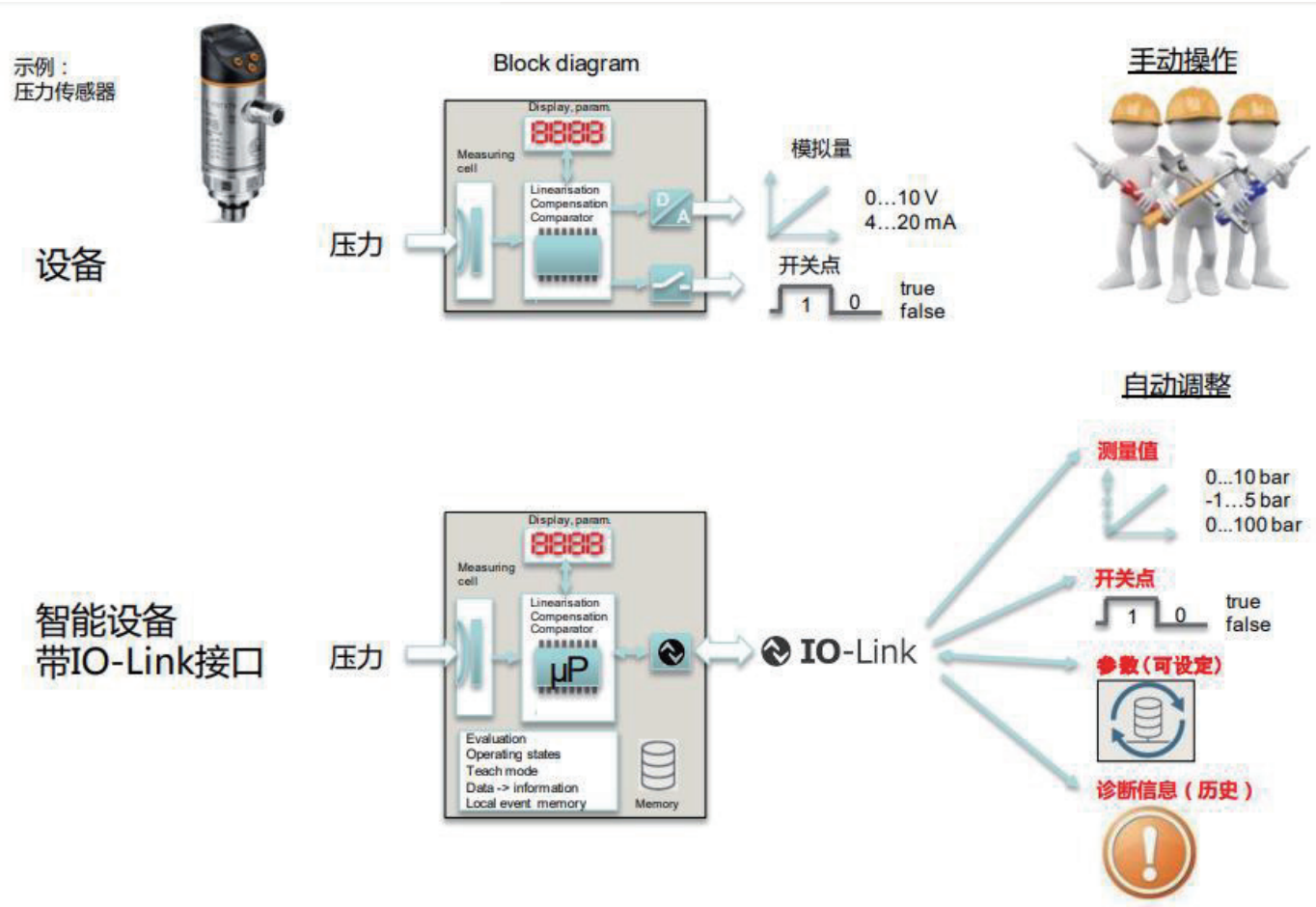
- 传感器和执行器可以直接与管理层级通信，并可以自动发出状态信号并生成警报。

- 如果需要，可以在本地乃至在全球范围内远程访问诊断或参数设置。

- 与现有自动化结构的集成很简单。

- 超过200家制造商遵循同一种协议！

IO-Link 系统构成



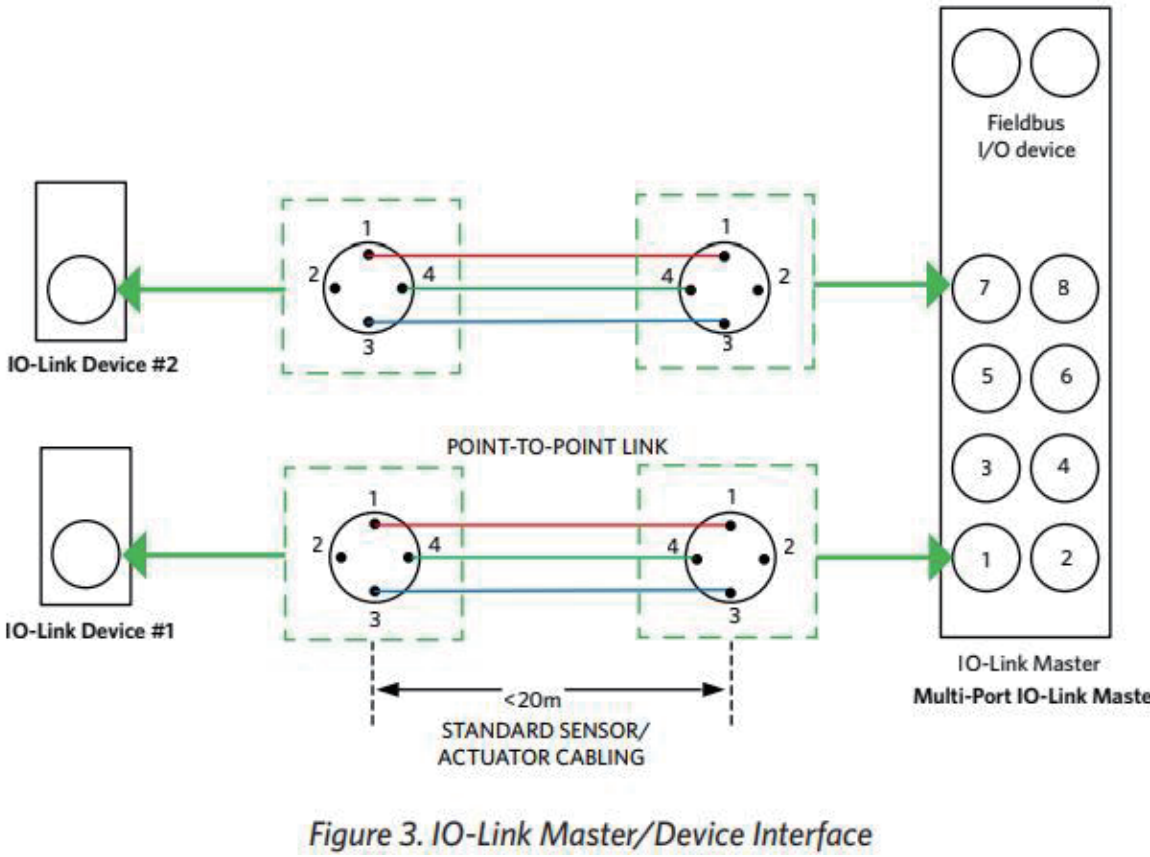


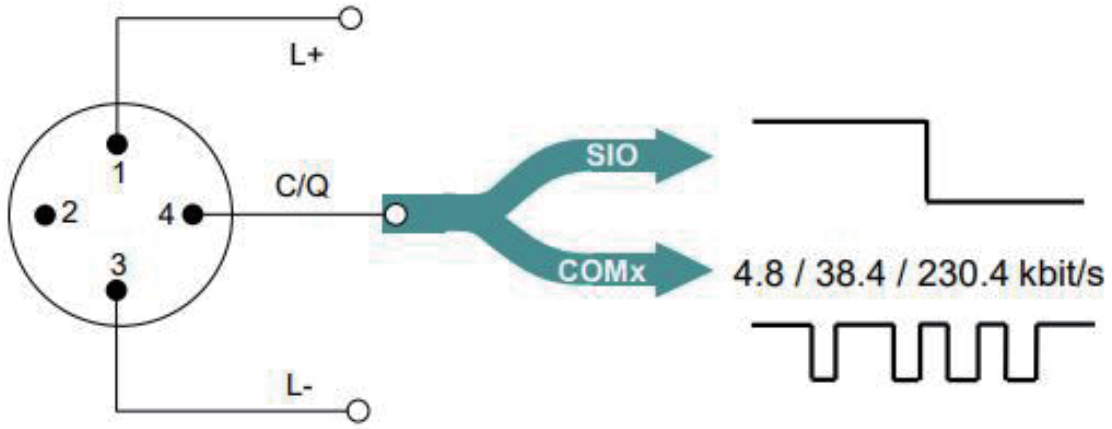
Figure 3. IO-Link Master/Device Interface

IO-Link系统由master、device构成，并由非屏蔽的3芯或5芯电缆连接。

对比传统IO硬接线，可以节省大量接线。

Note：M8/12航空插头极大增加IO-Link实用价值。

IO-Link是什么?



IEC 60947-5-2

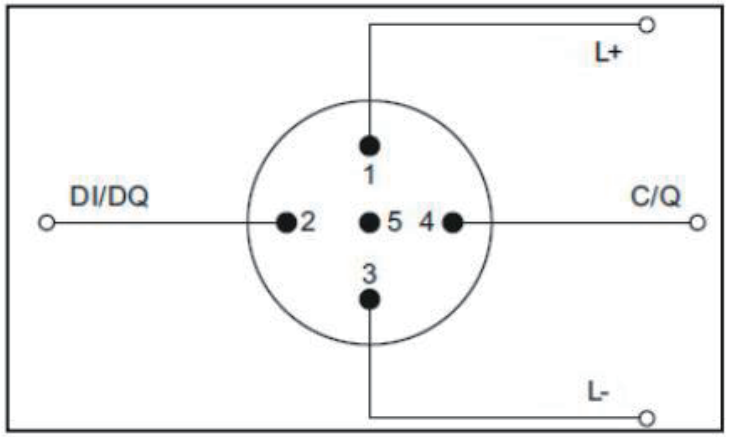


Figure 4: Pin assignment Port Class A

IO-Link是基于 IEC 61131-9的公开标准。

IO-Link是点对点通讯，不是现场总线！

IO-Link支持COM 1 = 4.8 kbaud, COM 2 = 38.4 kbaud COM 3 = 230.4 kbaud

IO-Link最远传输距离为20m.

IO-Link有两种接口形式： Class A 适用于信号仪表，Class B 适用于执行器

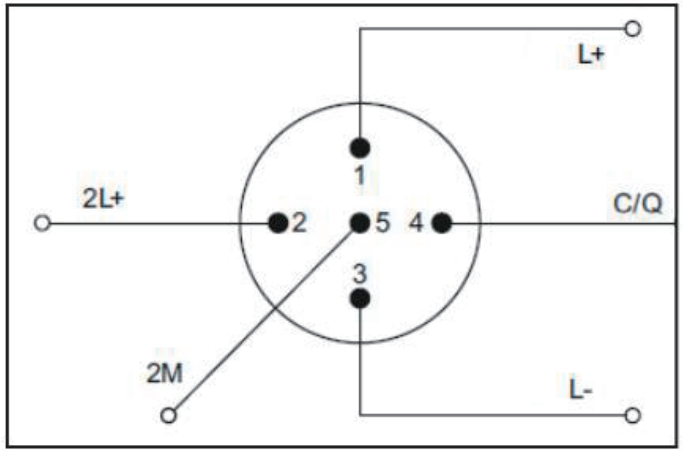


Figure 5: Pin assignment Port Class B

SDCI是什么?

SDCI Single-drop Digital Communication Interface,in part 9 of the IEC 61131

The (SDCI) Master function enables these peripherals to map SDCI Devices onto a fieldbus system or build up direct gateways. Thus, parameter data can be transferred from the PLC level down to the sensor/actuator level and diagnosis data transferred back in turn by means of the SDCI communication

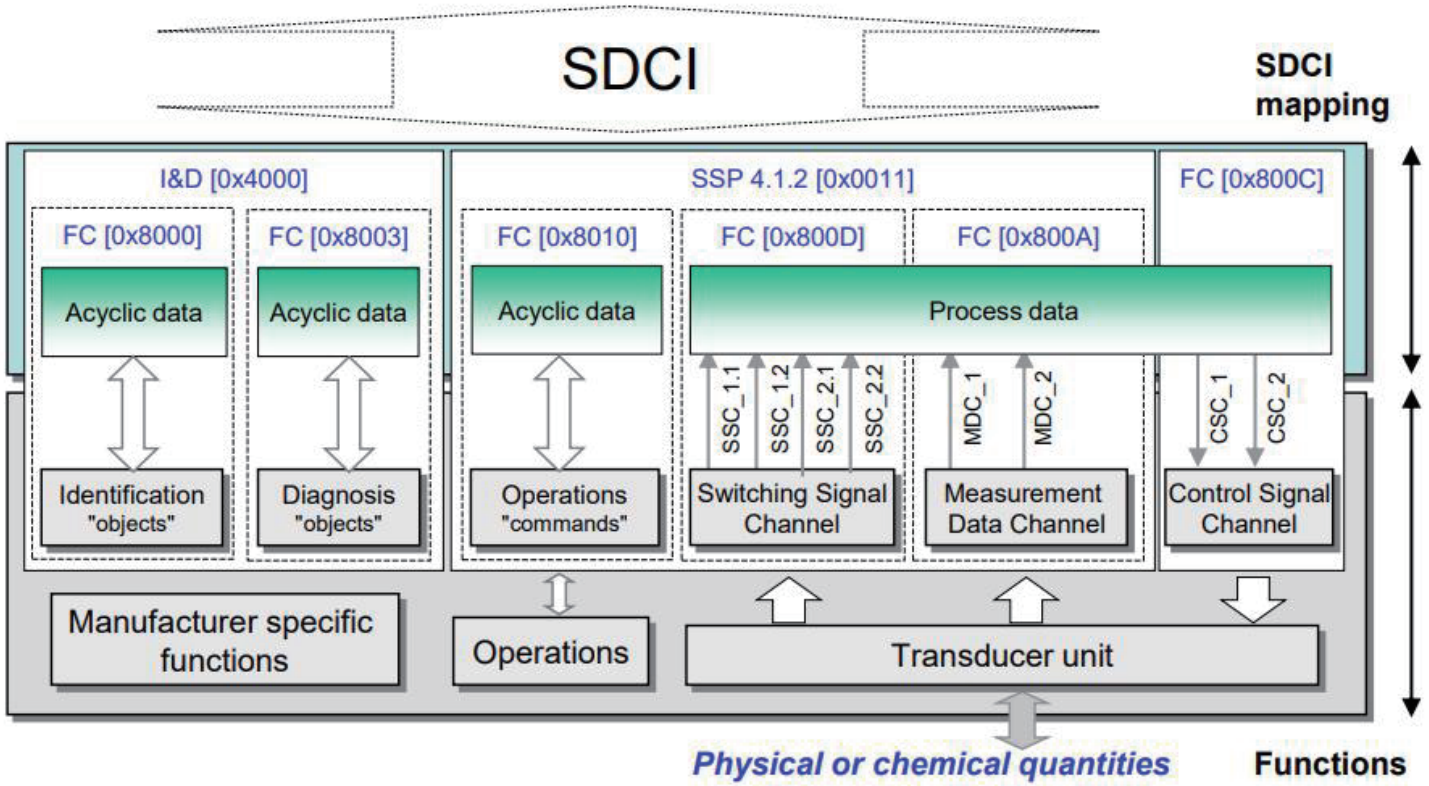


Figure 4 – Overview of typical FunctionClasses

Note:
通过PLC可以组态/配置IO-Link设备，这样，IO-Link无缝嵌入到现有的自动化技术中。
使用场景极大扩展!

SDCI与IO-Link的关系

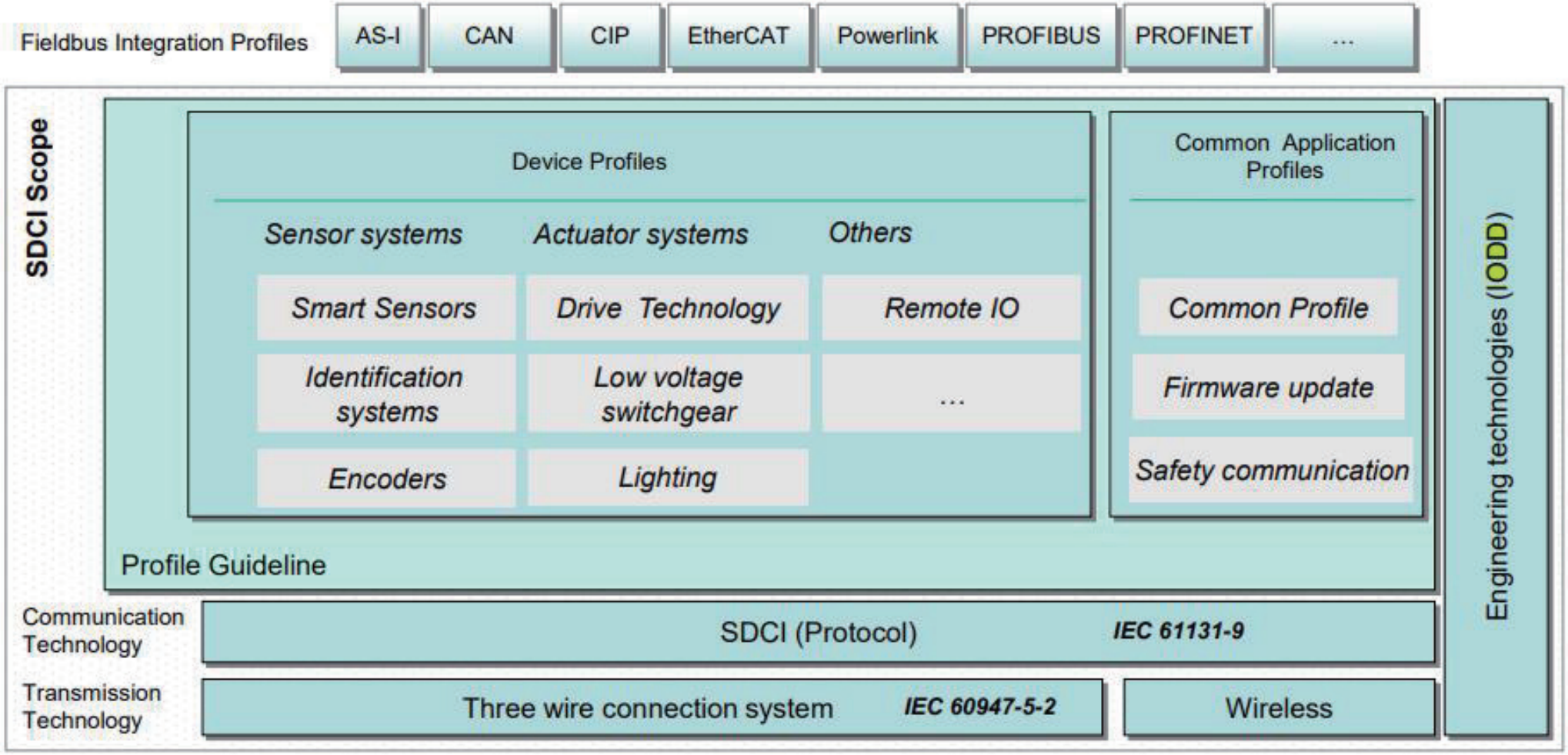


Figure 3 – Overview of SDCI technologies and profiles

IO-Link是system technology，包含了SDCI (IEC61131-9) 和Three wire connection system (IEC60947-5-2）)， 也包含Engineering technologies (IODD)和wireless.

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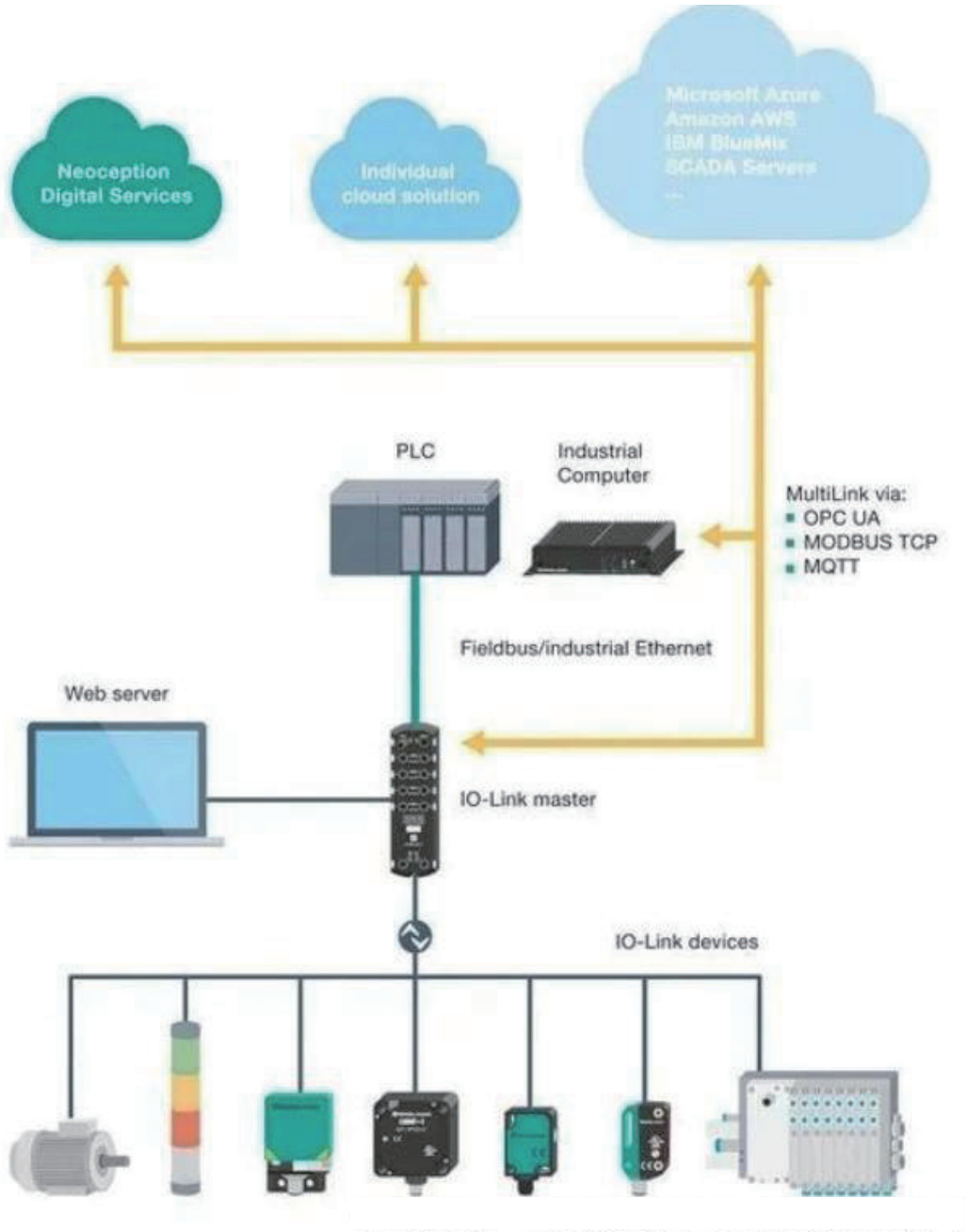
Y形链接，通往智能设备/智能工厂/工业4.0的桥梁



IO-Link既可以通过TIA/Codesys 整合进现有的自动化系统，

也可以通过OPC UA/MODBUS/MQTT接入工业云，应用到IIOT。

这种Y形链接，PLC仅获得5%的过程数值，IT信息层获得额外95%信息，如参数、诊断及事件。

同时，很多IO-Link master支持webserver，设备组态更加容易。

OPC UA for IO-Link Companion Specification Release 1.0

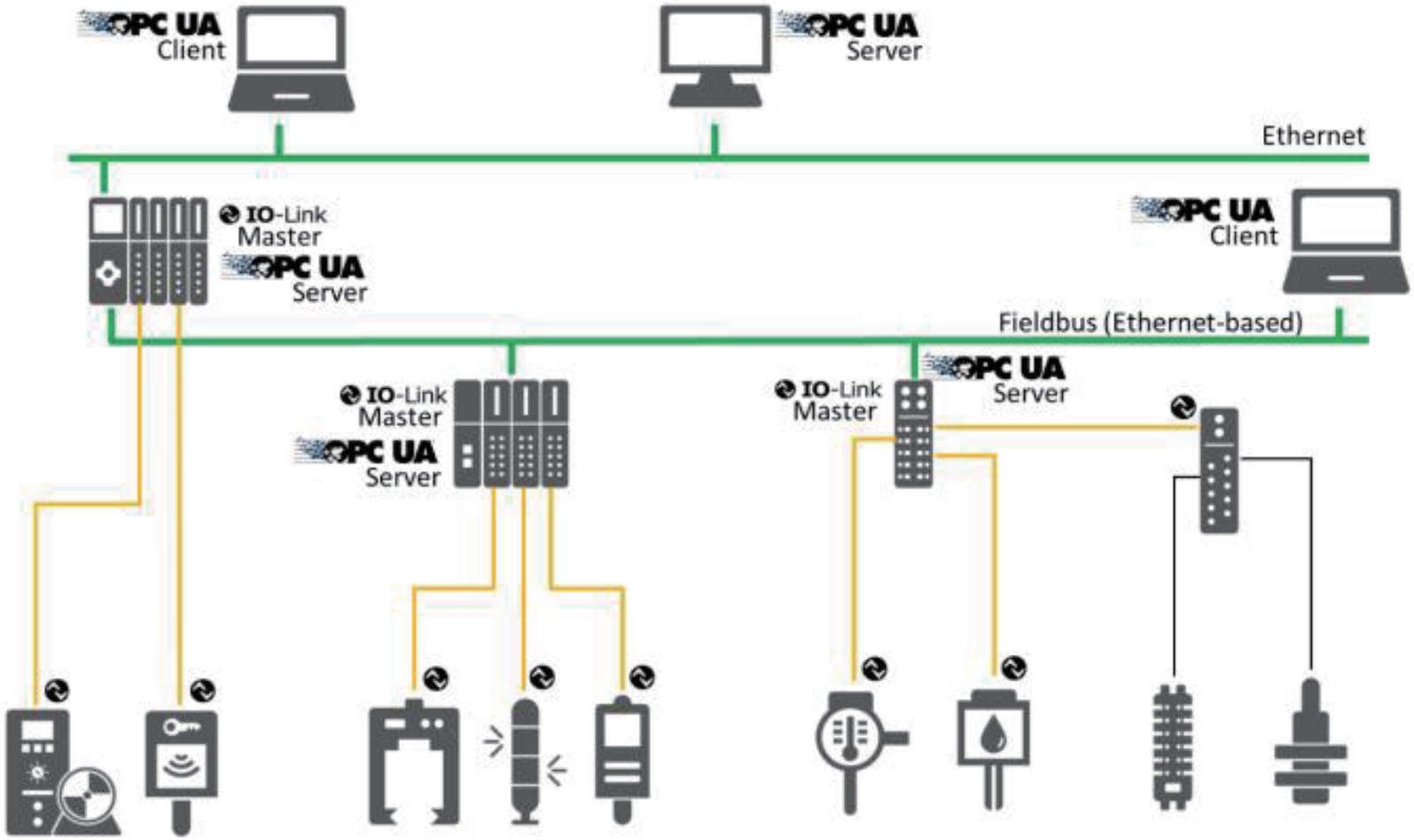


Figure 5 – System Architecture of IO-Link and OPC UA (Example)

OPC FOUNDATION IO-Link

IO-Link Community and OPC Foundation:

OPC Unified Architecture

for

IO-Link

Companion Specification

Release 1.0

December 01, 2018

IO-Link for Single Pair Ethernet(SPE) transmission

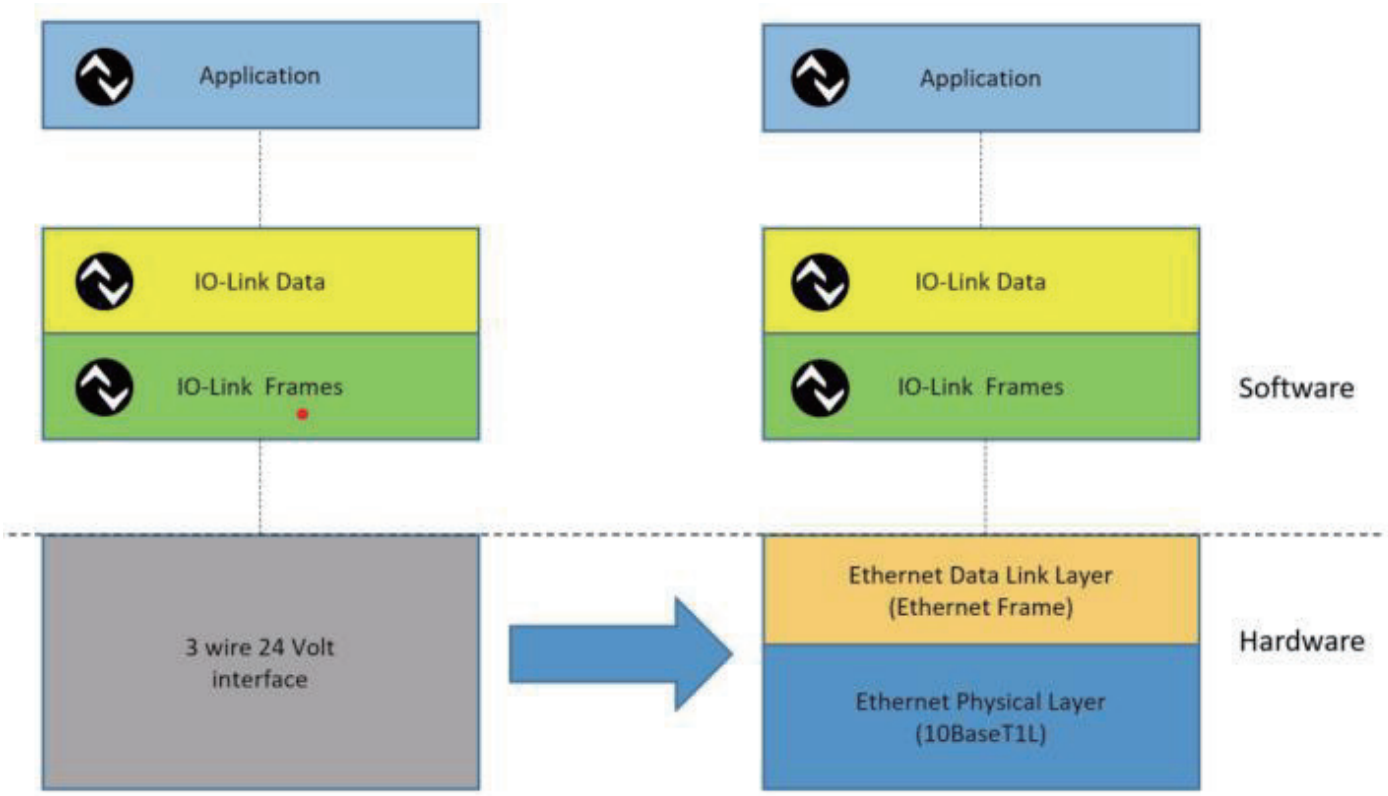
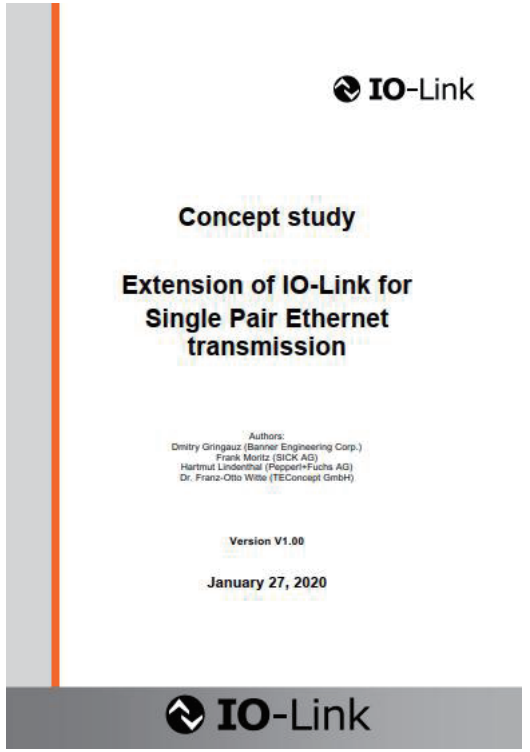
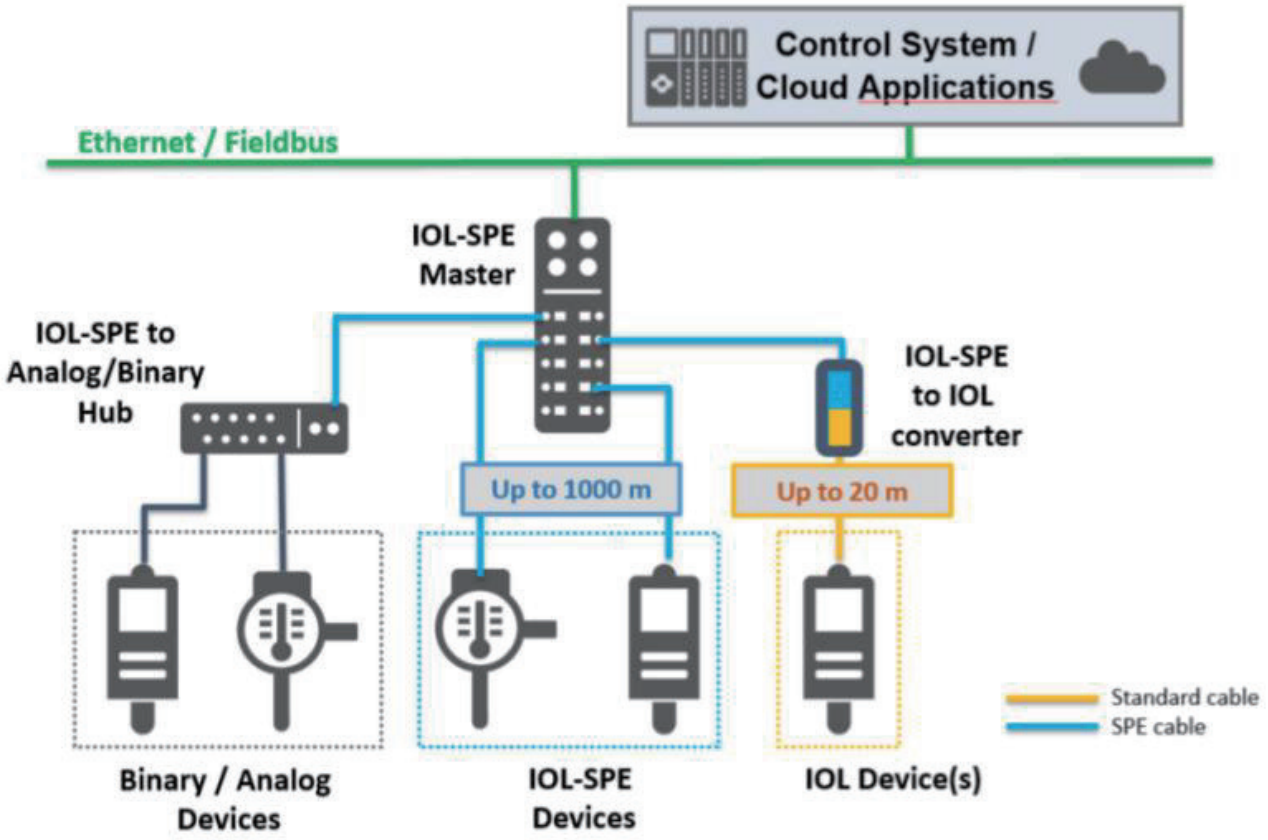


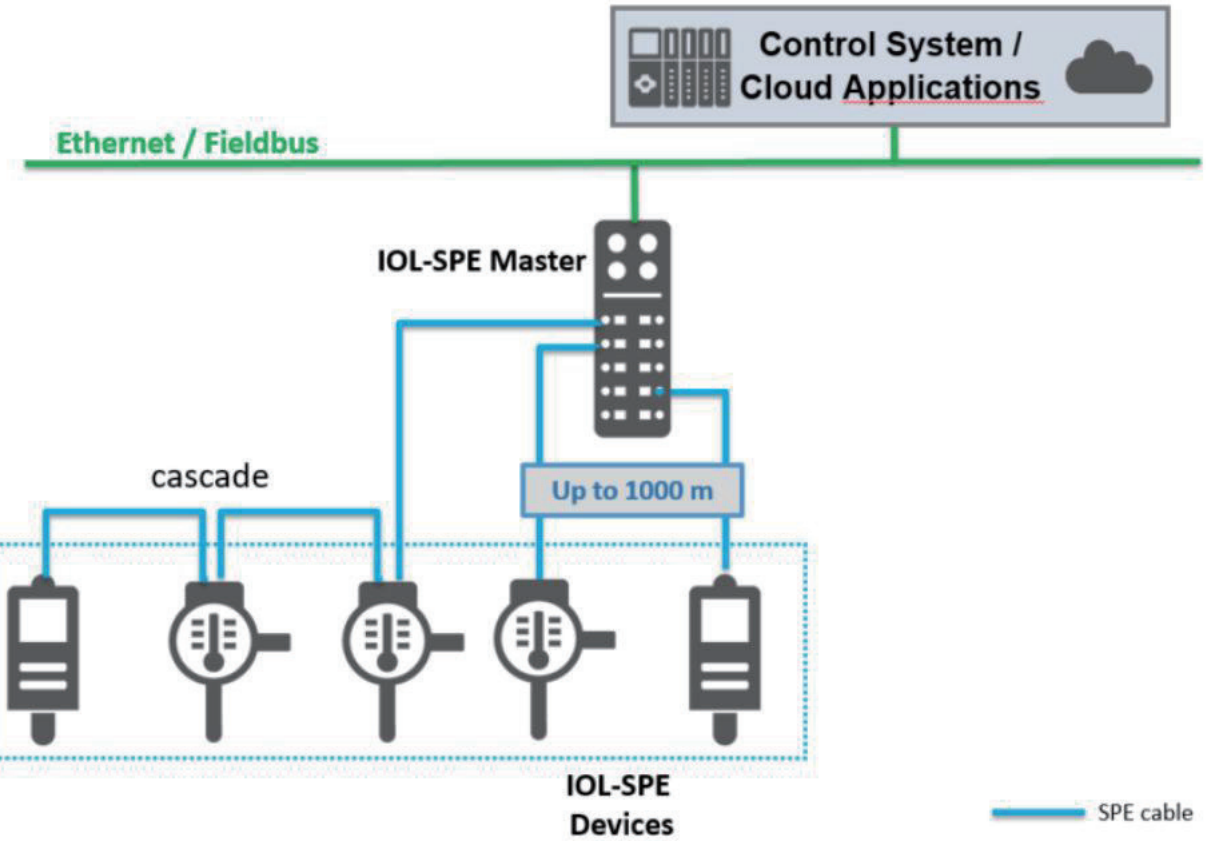
Figure 1 – Physical Layer modification



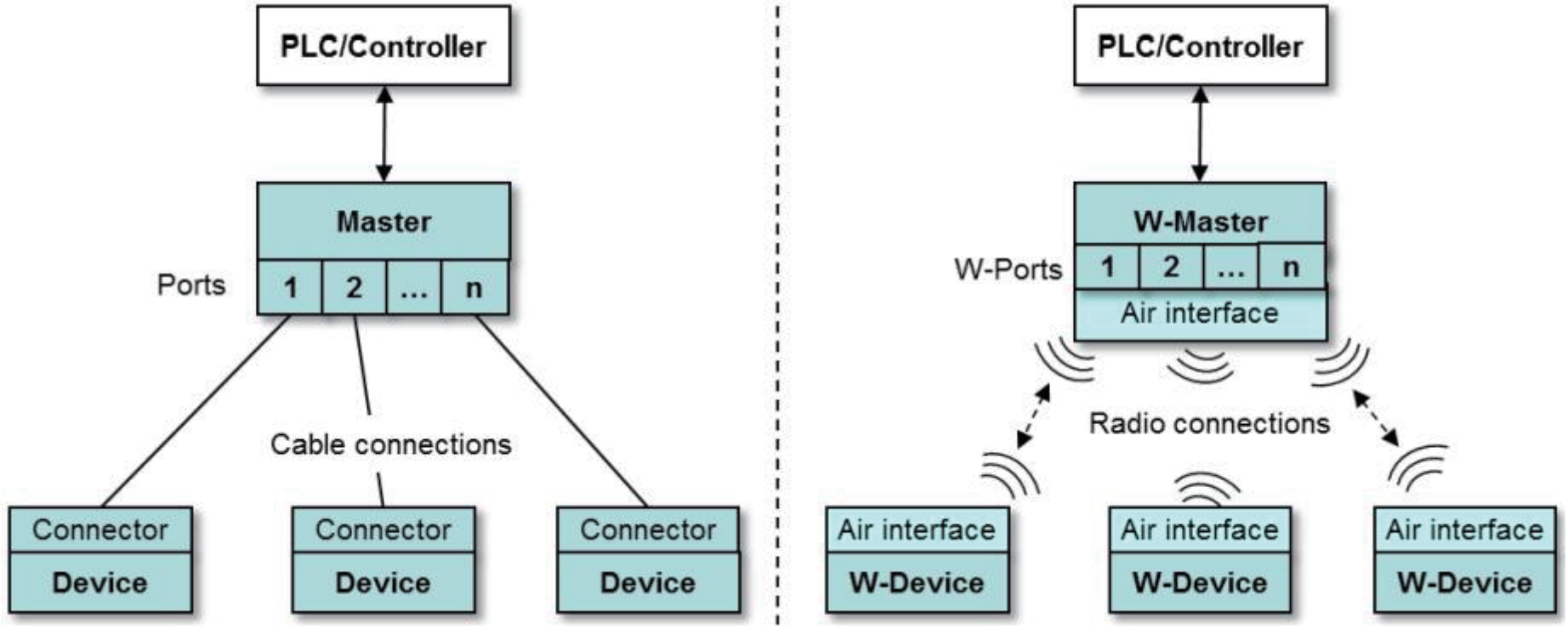
SPE，基于IEEE 802.3cg, 分为10BASE-T1L(长距离，双线)、10BASE-T1S（短距离，单线）、APL（本安，基于T1L）。Using 10Base-T1L for IO-Link。

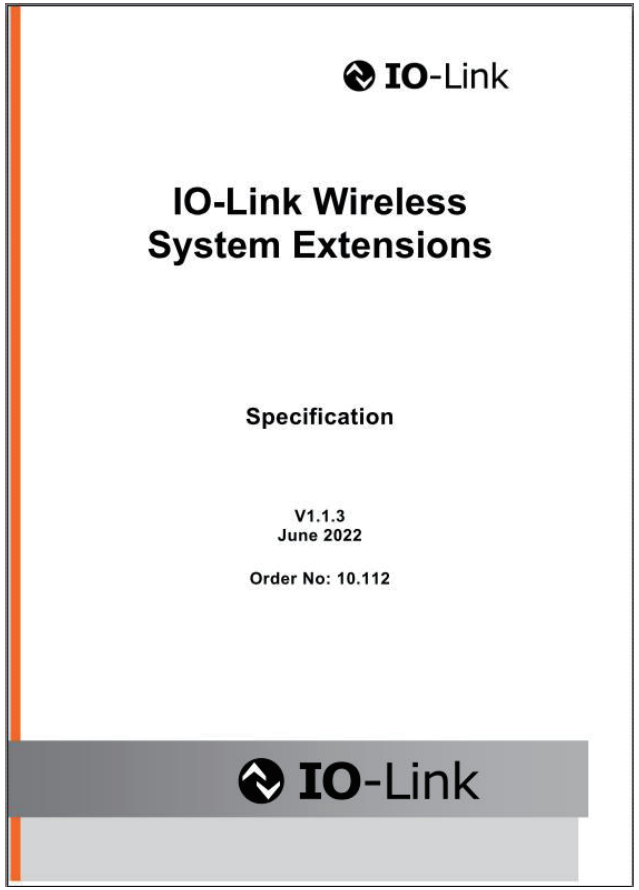
IO-Link over SPE





IO-Link Wireless





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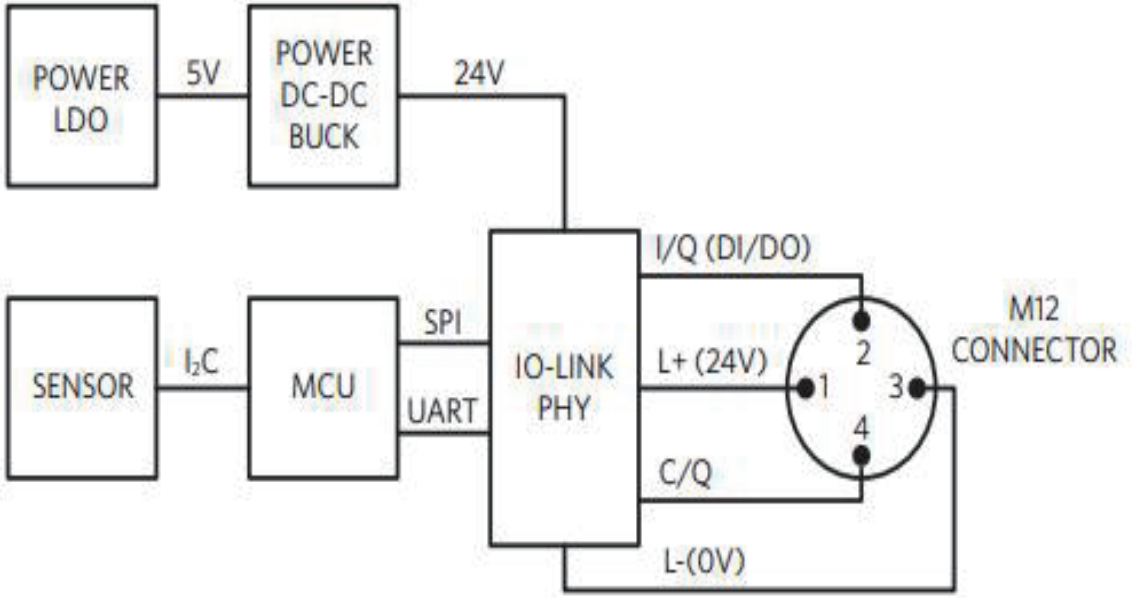
IO-Link Device解决方案

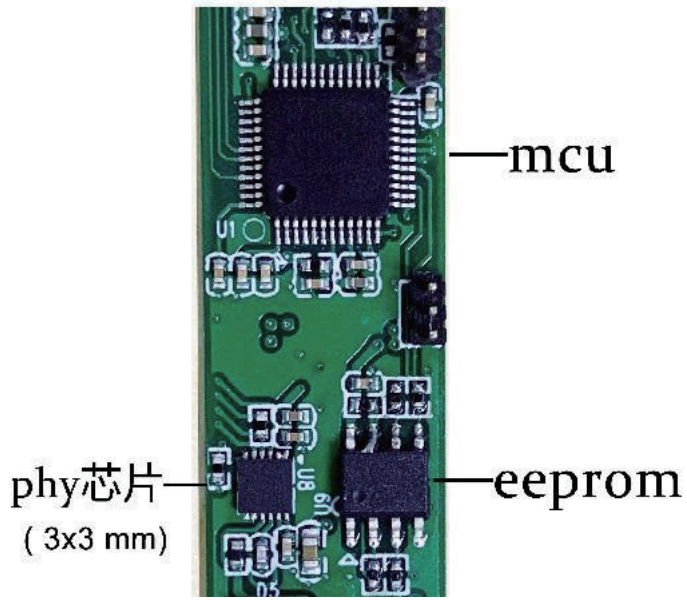
TEConcept

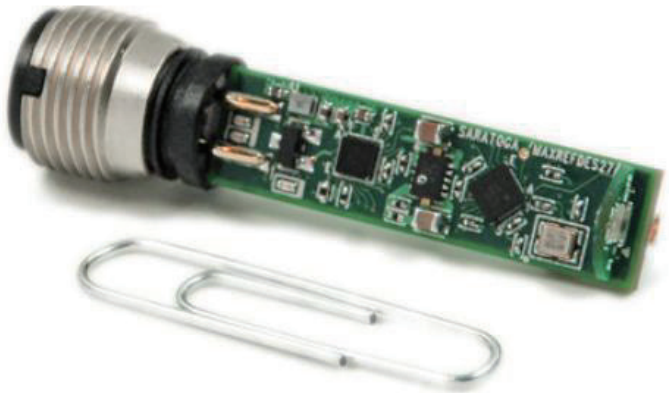
IO-Link

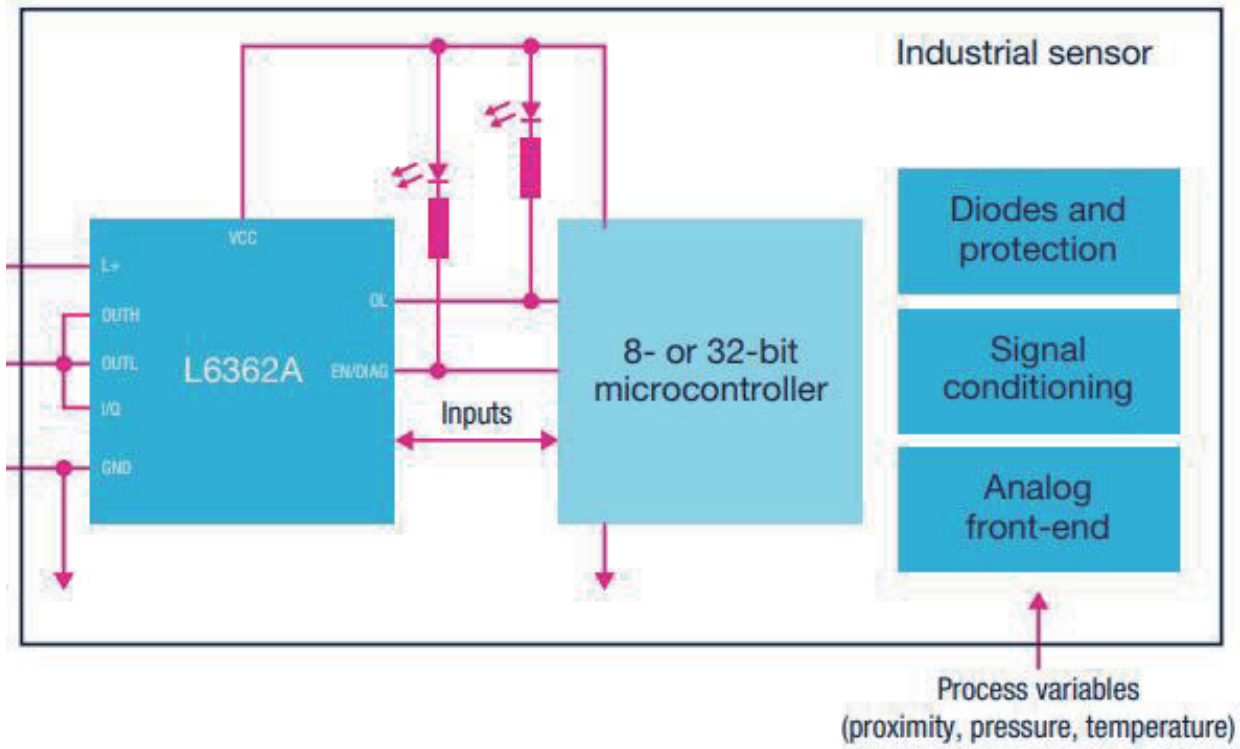
L6362A
DFN12L (3x3mm)



IO-Link Device开发案例

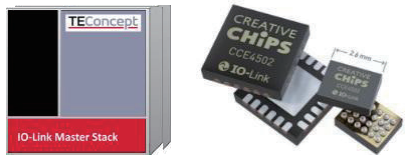






IO-Link 开发流程

启动	应用定义	设计	实施	测试	认证
• 协会会员 • 供应商ID • Device ID • 授权相关	• 应用(执行器，传感器) • 设备功能 • Sow	• 硬件 • 软件 • 测试	• PCB • 软件 • 结构 • HW/SW集成 • 原型机	• 应用测试 • 一致性测试 • 互操性验证 • Sow	• （测试中心） • 签署MD • （IO-Link project office报备（非会员））



硬件选型 协议栈

测试 改进

发布

IO-Link 开发准备

VELLEDQ® 为乐电气

会员

- IO-Link Vendor ID “VID” （16bit, PI-China）；
- 定义唯一Device ID “DID” （24bit）。制造商需要保证所有产品DID唯一性；
- 最新IO-Link规范；
- 相关授权许可。

非会员

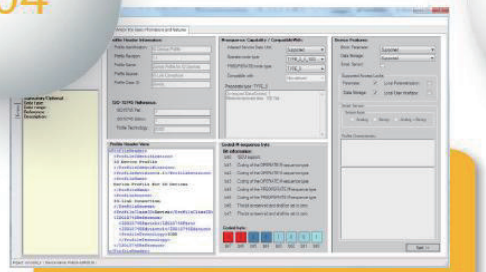
- IO-Link Vendor ID “VID” （16bit, PI-China）
- 定义唯一Device ID “DID” （24bit）。制造商需要保证所有产品DID唯一性；
- 从IO-Link Project officer获取用于IO-Link产品的文本和图片许可；
- 相关授权许可。

03

软件源代码

- IO-Link 协议栈...

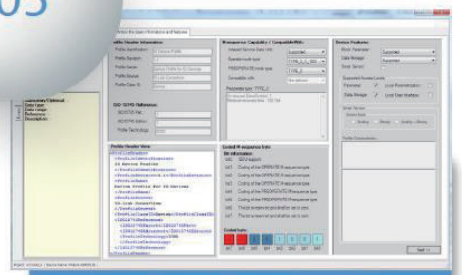
04



配置IODD

- 设备ID，设备名称，过程数据和配置数据数量...

05



测试

- 物理层测试、EMC测试...

IO-Link主站协议栈

IO-Link 主站协议栈

- 符合最新规范
- 多口支持
- 循环周期　　0,4ms @ 230,4 kBaud
  2,3ms @ 38,4kBaud
  18ms@ 4,8kBaud

- 源码形式的开发和制造授权
- 使用手册
- API手册
- 配置

Processor	PHY
STM32	L6360
ATSAM91	E981-12
LPC43xx	LT2874
Kinetis KL43/17	MAX14824
...	CCE4510
	CM3120

IO-Link 从站协议栈

IO-Link 从站协议栈

- 符合最新规范
- 过程数据同步、非同步处理
- ISDU
- 数据存储
- 大数据传输
- 业界最广泛的MCU PHY支持

Microcontroller	PHY
ADUC7xx	CCE4501
ATmega64/324/328	HMT7742
ATSAM3S	iC-GF
ATtiny	L6362A
C8051F31x/33x/37x/39x	LT3669-2
EFM32	MAX14820
Kinetis K02/K60	MAX14821
LPC11xx	SN65HVD101
MSP430	ZIOL2401
PIC32MXxxx	MAX14827A
RL78/xxx	MAX14828
STM32	
STM8L/STM8S	
... (to be continued)	

IO-Link 相关工具

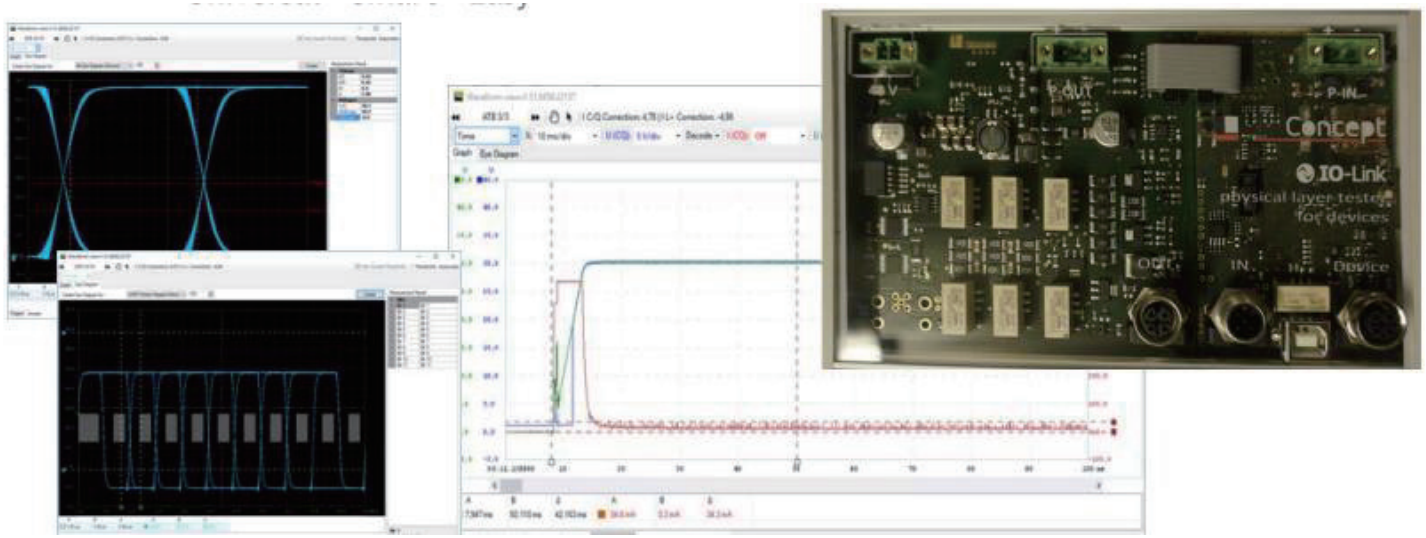
USB- 1 port Master

- Device Parametrization and Configuration
- USB and Serial and connection to PC
- Trace and Log
- Controlled by a simple PCT tool or a communication DLL
- Configuration storable
- Block parameterization
- Process data plotting
- UDP socket for process data handling
- User-Role, Menu support

IO-Link Diagnosis Tool

- Monitoring of IO-Link communication between ext. Master and device.
- Communication protocol in 4 levels
- Raw, M-Sequence, Protocol, IODD aware
- High speed waveform capture and display of voltage and current waveforms for C/Q and L+
- Accurate timing analysis
- Device response time, Bit-Timing
- Eye Diagrams of C/Q signal
- Process data plotting
- Internal Master for Device Testing
- Error logging

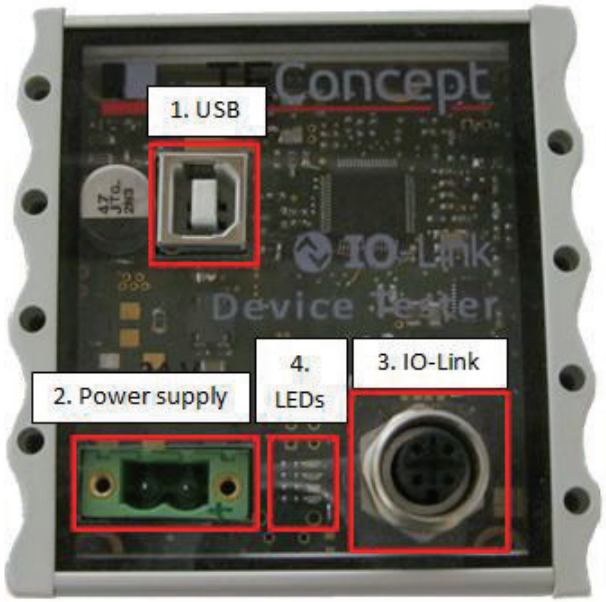
物理层测试



TEST CASE ATTRIBUTES	IDENTIFICATION / REFERENCE
Identification (ID)	SDCI_TC_009
Name	TCM_PHYL_INTF_IQPKHM
Purpose (short)	Test of high-side peak current driver capability, IQPKHM =
Equipment under test (EUT)	Master
Test case version	1.0
Category / type	Master Physical Layer; test to pass (positive testing)
Specification (clause)	[9], 5.3.2.3, table 6
Configuration / setup	The output level at the master C/Q output is measured.
TEST CASE	**CONDITIONS / PERFORMANCE**
Purpose (detailed)	Peak current driver capability of the master port high-side driver (wake-up request). Measurement of the voltage between negative supply L- and C/Q output. The driver shall drive a defined resistive load to a voltage level greater than the input high threshold level.
Precondition / prior test	Master set to SIO mode
Procedure	a) Apply minimum supply voltage (VSM = 20 V) to master b) Apply an equivalent resistive load Rload between C/Q and L- (Rload = VTHHDmax / IQPKMmin) *→ 13 V / 0,5 A = 26R → 51R||51R* c) Set Master to IO-Link-Mode (generate WURQ) d) Measure voltage VIM between negative supply L- and C/Q d) Check whether VIM is greater than the maximum limit of VTHHD (> 13 V) e) Repeat test with maximum supply voltage (VSM = 30 V)
Input parameter	-
Post condition / next test	-
TEST CASE RESULTS	**CHECK / REACTION**
Evaluation	The output level shall be within specified limits.
Test passed	Voltage VIM greater than or equal specification value of VTHHDmax (≥ 13,0 V)
Test failed	Voltage VIM less than specification value of VTHHDmax (< 13,0 V)
Results	VIM (VSM = 20 V): <value> VIM (VSM = 30 V): <value>

IO-Link 协议栈测试

协议测试



Device Test Report

IO-Link

SICK
Sensor Intelligence.

Vendor: SICK AG
Vendor ID: 0x001A

Device Name: Not specified
Device ID: 0x1030C7
Product ID: 1061063

IO-Link Version: 1.00
Bitrate: COM2
Min Cycle Time: 5000 µs

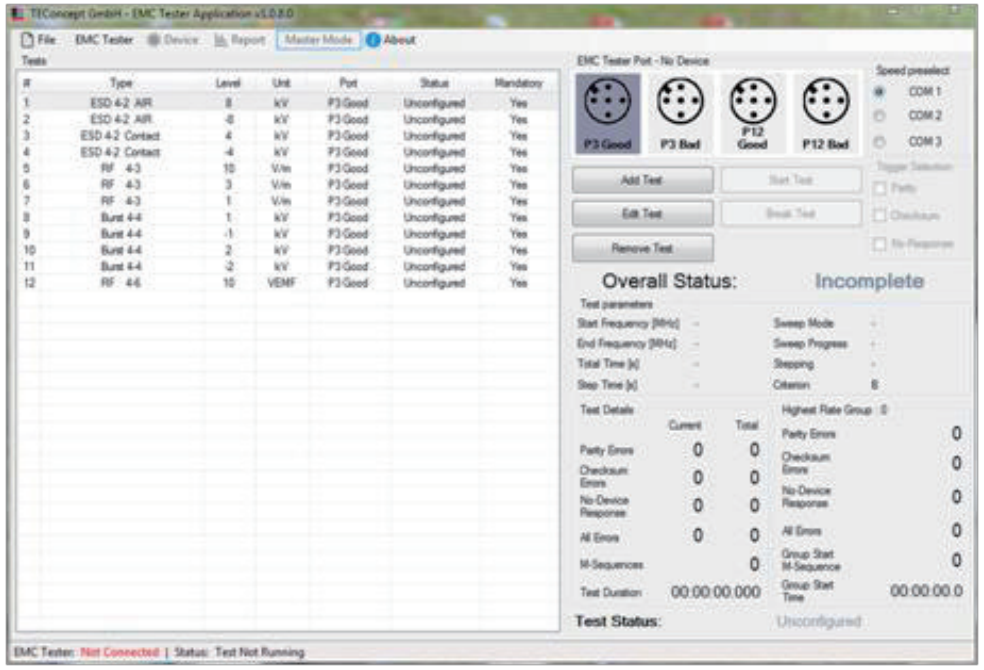
Process Data Input Bits: 16
Process Data Output Bits: 0

M-sequence capability: 0x01

SIO supported: yes
ISDU supported: yes
Data storage: no
Block parameters: no

IO-Link EMC测试

EMC测试



IO-Link 解决方案

VELLEDQ® 为乐电气

协议栈原代码

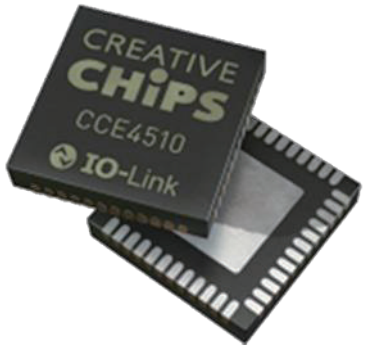
- 主站
- 从站

协议栈业务

开发工具测试工具

- IODDE编辑软件
- IO诊断工具
- IO-Link参数处理程序
- 物理层/协议栈/EMC测试工具

芯片业务



一致性测试服务

- 物理层/协议栈/EMC测试工具

THANK YOU

工业智能连接及保护解决方案